REMARKS

Claims 1-2, 8-18, and 23-25 are pending. Claims 11, 12, 23, and 24 are amended, claim 22 canceled, and new claim 25 is added with this response. New claim 25 includes all the limitations of previously presented base claim 1 and provisionally allowed claim 22, thus not introducing any new subject matter. Claim 23 and 24 have been amended to retain their respective original dependency on canceled parent claim 22, which now exists in the form of new claim 25, thus not introducing any new subject matter as well. Reconsideration of the application is respectfully requested in view of the following remarks.

I. REJECTION OF CLAIMS 11 AND 12 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 11 and 12 were rejected under 35 U.S.C. 112, as failing to provide sufficient antecedent basis. Withdrawal of this rejection is requested for at least the following reasons.

Claims 11 and 12 have been amended to include proper antecedent basis, as suggested by the Office Action dated October 3, 2008. Accordingly, withdrawal of this objection is respectfully requested.

II. REJECTION OF CLAIMS 1, 2, AND 8-12 UNDER 35 U.S.C. § 102 (e)

Claims 1, 2 and 8-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,185,438 (Fox). Withdrawal of this rejection is requested for at least the following reasons.

i. Fox does not teach a data packet located in an array of virtual buffers that each map to one or more physical buffers in a system memory, as recited in claim 1.

Claim 1 is directed to a method for partial coalescing transmit buffers. The method comprises obtaining a data packet from host software, ***wherein the data***

packet is located in an array of virtual buffers that each map to one or more physical buffers in a system memory. Fox does not teach this feature.

Fox discloses a communication processor that uses a group of hardware buffer descriptors and a virtual array of buffer descriptors to control the communication ports of the communication processor. (*See* Abstract). ***The buffer descriptors, of Fox, that control the communication ports of the communication processor, store status and control information about the communication ports and the data being communicated.*** (*See, e.g.*, Col. 1, line 58- Col. 2, line 3). The status and control information about the communication ports and the data being transmitted and received includes:

1.) The starting address of the data buffer holding the needed data.
2.) The length of the data in the data buffer.
3.) The bits that may be used to activate and deactivate the digital processor or to indicate certain conditions, including errors.

(*See, e.g.,* Col. 2, line 64-Col. 3, line 3)

Because of a limitation on the number of registers to be used as buffer descriptors, as taught by Fox, the throughput of the base transceiver station is limited because the buffer descriptors are used to control communication ports. (*See, e.g.*, Col. 2, lines 6-15). When the buffer descriptors of a digital processor are filled and additional data packets are available for processing/transmission, ***the data packet must wait unit a buffer descriptor becomes available to store them. (It is to be duly noted that the use of "them" is implicitly defined as storing the status and control information about the communication ports and the data packets, considering this is the only data that is operable to be stored in a buffer descriptor, as taught by Fox).*** As will be further appreciated from the following discussion, the hardware buffer descriptor or

the virtual array of buffer descriptors ***do not store data packets***, contrary to what is recited in claim 1 of applicant.

The Office Action recites, "...obtaining a data packet from host software, wherein the data packet is located in an array of virtual buffers that map to one or more physical buffers in a system memory..." is recited by Fox (*See, e.g.,* Col. 2 lines 49-60, Col. 7 lines 16-27 and 40-51). Applicant respectfully disagrees with the interpretation of the reference and offers this clarification to the teaching. Fox teaches (*See, e.g.,* Col. 2 lines 49-60) the communication processor under the control of application software takes outbound data from a receiver port or from other data sources in, or connected to, the transceiver controller and fills the transmitter virtual array of buffer descriptors and sets the control bits. Fox further teaches an interrupt controller detects an emptiness condition and moves the contents of the transmitter virtual array of buffer descriptors to the hardware transmitter buffer descriptors, which allows for the virtual array of buffer descriptors to be cleared and the control bits to be reset, thus allowing further incoming data to be stored in the transmitter virtual array of buffer descriptors. Special consideration is to be given to the definition of the ***data*** that is to be stored in the transmitter virtual array of buffer descriptors, as taught by Fox. The ***data stored in a virtual array of buffer descriptors, as outlined above, is only status and control information*** for the transmission or reception of data packets by the processor communication port. Therefore it is clearly apparent, that Fox does not teach or suggest a ***data packet*** that is located in an array of virtual buffers, as recited in claim 1 of applicant.

The Office Action further cites Fox (*See, e.g.,* Col. 7, lines 16-27 and 40-51) in teaching "...obtaining a data packet from host software, wherein the data packet is located in an array of virtual buffers that map to one or more physical buffers in a system memory...". However, this subsequent reference does not teach the claimed feature of the applicant either. Fox teaches (*See, e.g.,* Col. 7, lines 16-27 and 40-51, Figure 4) Virtual Array Buffer Descriptor (VABD) 370 are logically subdivided into VABD table 371 that is arbitrarily labeled "VTBD1" through "VTBDn" for the virtual transmit

buffer descriptors and "VRBD1" through "VRBDn" for the virtual receive buffer descriptors where "n" and "m" are indices. Each of VTBD1-VTBDn or VRBD1-VRBDm ***points to a location in transmit data buffer 350 or receive data buffer 360 where the outbound or inbound data are stored, respectively***. This teaching of Fox confirms that ***the data packets are stored in data buffers 350 or 360 and not in the buffer descriptors***. Therefore, Fox does not teach or suggest a data packet that is located in an array of virtual buffers, as recited in claim 1 of applicant.

It is concluded from the teaching of Fox, a data packet is never stored in an array of virtual buffers but is stored in data buffers 350 and 360. Additionally Fox does not teach of an array of buffers but teaches of an array of virtual buffer descriptors.

Therefore independent claim 1 along with respective depending claims 2 and 8-12 are believed not anticipated by Fox and thus allowable. Accordingly withdrawal of the rejection is respectfully requested.

III. ALLOWABLE SUBJECT MATTER

Allowance of claims 13-18 is noted with appreciation.

IV. NEW CLAIM 25

Claim 25 is added herein and is believed to be allowable over the cited reference. Claim 25 includes all the limitations of previously presented base claim 1 and provisionally allowed claim 22, thus not introducing any new subject matter.

II. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP772US.

Respectfully submitted,
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